

# AN UNBALANCED CLOCK BASED DYNAMIC COMPARATOR: A HIGH-SPEED LOW-OFFSET DESIGN APPROACH FOR ADC APPLICATIONS

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**Abstract.** Currently, dynamic comparator approach necessitates in high-speed and power efficient analog-to-digital converter applications due to its high latching speed and ultra-low power consumption. In this paper, a novel dynamic comparator is proposed to reduce latch delay and offset. The comparator benefits from add-on cross-coupled transistors in latch structure and unbalanced clocks to enhance comparison speed and to lessen input offset voltage occurred due to mismatch in cross-coupled circuits in latch stage. The derivations for delay and input offset voltage are presented for proposed dynamic comparator with meticulous Monte-Carlo simulations. The results are verified by simulations in CADENCE SPECTRE at 1 V supply voltage and 90 nm CMOS technology. A comparative analysis between the proposed dynamic comparator and the previous reported comparators has been presented. It is observed that the delay is reduced up to 46 % and 6 % as compared to conventional and two phase dynamic comparator, respectively. Moreover, the proposed design consumes 53.36  $\mu$ W power only. The Monte-Carlo simulation shows that the standard deviation of input offset voltage is 10.8 mV which is 12 % and 77 % of conventional and two phase dynamic comparator, respectively.

## Keywords

*Dynamic comparator, high speed, latch comparator, low offset design, unbalanced clock.*

## 1. Introduction

For past few decades, the regenerative latch circuits in comparators have been playing a vital role as interface between digital and analog signals [1]. It is a main

building block that is widely used in a variety of systems such as Analog-to-Digital Converters (ADCs) [2], memory devices [3] and [4], Variable Gain Amplifiers (VGAs) [5] or switched capacitor circuits. High switching speed, low offset [6] and [7] and energy efficient [8] comparators having small die area are required for flash type ADCs. But trade-off between speed, offset and power makes it challenging to design high speed low offset comparators [6]. In recent CMOS processes, high speed comparators suffer from low voltage supply in Ultra-Deep Submicron (UDSM) CMOS technology because the threshold voltage is not scaled in same way as supply voltage [9], resulting in limitations on voltage headroom and common mode input voltage range. A challenge towards high speed low power comparator is increase of kickback noise [10] and offset caused by mismatches due to threshold voltage, capacitances, and current factors. Thus, this major thrust to design high performance comparators is a huge challenging task in ADC design environment.

Comparators are classified as static and dynamic depending on the clock signal. Static comparators [10] suffer from static power dissipation and are not suitable for high speed low power applications. Best suited comparators for high speed operations are dynamic comparators having no static power dissipation [11]. However, this topology creates stacking effect and fails for low voltage applications because appropriate delay time requires proper voltage headroom [12]. Many researchers have introduced a lot of techniques to design comparators such as body driven technique [13], [14] and [15], charge steering technique [16], Zero- $V_t$  MOS based technique [17], offset cancellation technique [15], [18], [19] and [20], shared charge method [21], and supply voltage bootstrapping and boosting [22] and [23] method to meet the above requirements. In body-driven technique [13], the thresh-

old voltage requirement is removed due to MOSFET operation in depletion mode, but it suffers from lesser trans-conductance in comparison of gate driven technique. Also, for both PMOS and NMOS operation in body driven design, a unique fabrication process as  $n$ -well is required. The comparator, based on Zero- $V_t$  devices [17] provides rail-to-rail input range and fast switching at low supply voltage. However, Zero- $V_t$  devices in many CMOS processes are not available, and fabricate them physically is impossible. So, above mentioned techniques are not unswerving for low voltage applications in spite of being effective. To remove stacking effect in [9] and [12], an extra circuitry is added to conventional comparator to increase speed in UDSM low voltage supply. In this approach, additional circuitry creates component mismatch which should be considered. To overcome all these challenges, double-tail two stage dynamic comparators [24], [25] and [26] comprising separate amplification stage and regenerative stage are proposed for energy efficient and lesser delay. By including some extra circuitry [25], power consumption is reduced in the expense of delay and area. To enhance regenerative speed, a new quasi-dynamic [8] regenerative stage is proposed, but static power dissipation occurs in amplification stage.

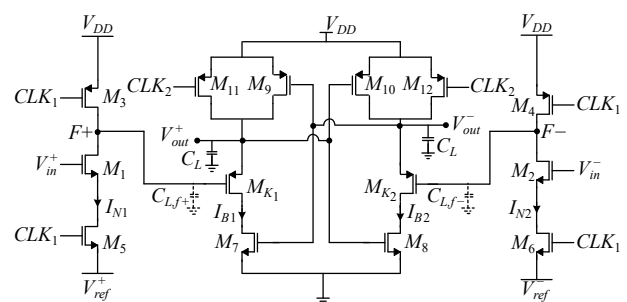
A classical single phase comparator named as "Lewis-Gray" comparator was introduced in [27] and [28] to explain compromise in offset, delay and power. It is widely used in ADC systems [28], therefore is taken as reference in this paper. It is fully differential dynamic comparator and consists of pre-amplifier stage and regenerative latch stage like other single phase comparators. When pre-amplifier stage develops sufficient voltage difference at the inner nodes of latch stage, it starts comparison and functions properly. In [29], an analysis of input offset voltage shows that it can be diminished on the cost of higher power consumption. At the regeneration phase amplification of input voltages and regeneration of cross-coupled inverters occur concurrently. Therefore, amplification should be quick and sufficient to suppress offset of cross-coupled inverters which leads to more power consumption. At the output node, load capacitance mismatch again affects input offset which needs more controlling input stage. To break this stalemate between power and offset, a new double phase based architecture [30] was introduced with significant lesser input offset with less power penalty. Nevertheless, a penalty on delay occurs.

In this paper, an improved unbalanced clock based dynamic comparator has been proposed in which an extra circuitry is included in latch stage as cross-coupled transistors. Now, output nodes of pre-amplifier stages are passed to intermediate transistors in place of direct connected with output nodes of latch stage that improves the performance of the proposed comparator.

A significant delay is reduced without penalty on offset and power consumption but on the cost of some area caused by extra circuitry. The remnant of this paper is structured as follows: In Sec. 2, the proposed comparator is explained along with mathematical analysis of delay and input offset. In Sec. 3, design considerations are explained in which some design issues are elaborated. Simulation results are discussed and compared with past designs in Sec. 4. whereas Sec. 5. concludes the paper.

## 2. Proposed Comparator

The proposed comparator, shown in Fig. 1, is composed of two stages: 1) pre-amplification stage and 2) regenerative latch stage. Pre-amplification stage is formed by transistors  $M_1$ ,  $M_2$ ,  $M_3$ ,  $M_4$ ,  $M_5$ , and  $M_6$ , where  $M_1$  &  $M_2$  are input transistors and rest are controlled by clock  $CLK_1$ . Regenerative latch stage is formed by transistors  $M_7$ ,  $M_8$ ,  $M_9$ ,  $M_{10}$ ,  $M_{11}$ ,  $M_{12}$ ,  $M_{K_1}$ , and  $M_{K_2}$ , where  $M_7/M_9$  &  $M_8/M_{10}$  transistor pairs set up a latch together and  $M_{11}$  &  $M_{12}$  are controlled by clock  $CLK_2$ . It has been depicted that latch effective trans-conductance,  $g_{m,eff}$  and differential output voltage at the start of comparison phase,  $\Delta V_0$  affect the total delay time of comparator. To enhance effective trans-conductance of latch stage and latch speed, two intermediate transistors  $M_{K_1}$  &  $M_{K_2}$  are included in latch stage which in turn enhancing  $\Delta V_0$  resulting lower delay.

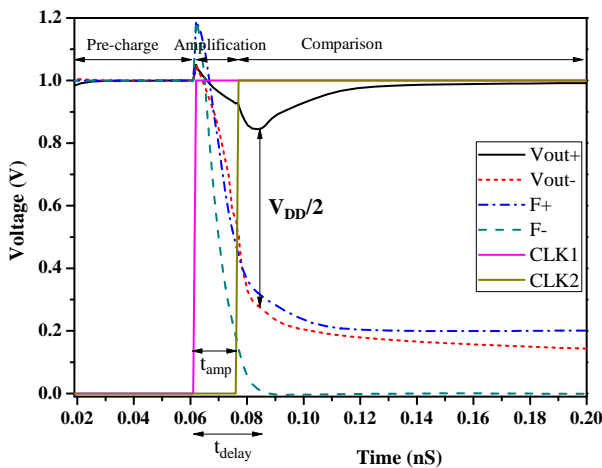


**Fig. 1:** Proposed unbalanced clock based dynamic comparator.

The two separate stages, i.e. regenerative latch stage and pre-amplification stage function with two clock pulses  $CLK_1$  and  $CLK_2$  individually. These clocks aid the input transistors to reduce the mismatch effect in the latch stage. Thus, the input offset voltage of comparator is reduced significantly. This circuit has less stacking, so it can operate at low supply voltage.

## 2.1. Operation of Proposed Circuit Architecture

The proposed comparator functions with the three phase operations: pre-charge, amplification and comparison phase as illustrated in Fig. 2. During the first phase when both the clocks  $CLK_1$  and  $CLK_2$  are low, the transistors  $M_3$ – $M_4$  pre-charge the nodes  $F+$  and  $F-$  causing  $M_{K1}$ – $M_{K2}$  to be off and  $M_{11}$ – $M_{12}$  transistors pull the output nodes  $V_{out}^+$  and  $V_{out}^-$  to  $V_{DD}$ . In second phase,  $CLK_1$  is high, however  $CLK_2$  is still low. Now, the nodes  $F+$  and  $F-$  start to discharge and an input and reference dependent differential voltage  $\Delta V_{F+/F-}$  is developed due to differential current produced in input branches  $I_{N1}$ – $I_{N2}$ . The intermediate transistors  $M_{K1}$  and  $M_{K2}$  pass  $\Delta V_{F+/F-}$  to cross-coupled inverters that provides good shielding between input and output. Hence, kickback noise is reduced. A sufficient differential voltage is developed at the output nodes of the latch stage which is related to differential input and reference voltages. The clock  $CLK_2$  is set to high during third phase, resulting latch circuit starts to operate. The regenerative loop of back-to-back inverters boosts the developed differential voltage at output nodes. Assuming  $V_{in}^+ > V_{in}^-$ ,  $V_{out}^+$  discharges faster than  $V_{out}^-$ . Consequently, when  $V_{out}^+$  (discharged by  $M_{K1}$  drain current) falls down to  $V_{DD} - |V_{thp}|$  before  $V_{out}^-$  (discharged by  $M_{K2}$  drain current), the corresponding transistor  $M_{10}$  will be ON instigating comparison phase.  $V_{out}^-$  pulls back to  $V_{DD}$  and  $V_{out}^+$  discharges to  $V_{thp}$  due to PMOS intermediate transistors. If  $V_{in}^+ < V_{in}^-$ , the circuit works vice-versa.



**Fig. 2:** Proposed unbalanced clock based dynamic Transient response of the proposed comparator for the differential input voltage,  $\Delta V_{in} = 5$  mV, supply voltage,  $V_{DD} = 1$  V and common mode voltage,  $V_{CM} = V_{DD}$ .

## 2.2. Delay Analysis

In order to validate delay reduction mathematically, the delay equations are derived for this proposed circuit as presented in [21] and [24]. The total delay consists two parts: amplification phase duration,  $t_{amp}$  and regenerative latch stage delay,  $t_{latch}$ .

$$t_{delay} = t_{amp} + t_{latch}. \quad (1)$$

The delay  $t_{amp}$  is the time duration in the amplification phase when the latch stage load capacitance  $C_L$  at output nodes discharges until the first PMOS ( $M_9/M_{10}$ ) turns on. Here, the first PMOS ( $M_9/M_{10}$ ) will turn on when first preamplifier output node ( $F+/F-$ ) will discharge from  $V_{DD}$  to  $(V_{DD} - V_{thp})$  [24]. Thus,  $C_L$  is discharged by  $V_{thp}$  in  $t_{amp}$  time duration. Hence,  $t_{amp}$  is obtained as:

$$t_{amp} = \frac{C_L \cdot \{V_{DD} - (V_{DD} - |V_{thp}|)\}}{I_{B1}}, \quad (2)$$

$$t_{amp} = \frac{C_L \cdot |V_{thp}|}{I_{B1}} = \frac{2C_L \cdot |V_{thp}|}{I}, \quad (3)$$

where  $I_{B1}$  is the drain current of  $M_{K1}$ . Let, sum of  $I_{B1}$  and  $I_{B2}$  currents (i.e.  $I_{B1} + I_{B2}$ ) is equal to total supply current  $I$ , then  $I_{B1}$  can be approximated as half of supply current  $I$  for small differential input ( $\Delta V_{in}$ ).

If  $\Delta V_0$  is the initial output voltage difference at the beginning of comparison phase, latch delay can be obtained from [31]:

$$t_{latch} = \tau \cdot \ln \left( \frac{V_{DD}}{\frac{\Delta V_0}{2}} \right), \quad (4)$$

where  $\tau = C_L/g_{m,eff}$  in which  $g_{m,eff}$  is the effective trans-conductance of the cross-coupled inverters. From Eq. (4), it is clear that speed of proposed comparator can be improved by enhancing  $\Delta V_0$  and  $g_{m,eff}$ .

- **Enhancement in  $\Delta V_0$ :** As discussed earlier,  $t_{amp}$  is the time after which comparison phase starts and one of the latch output charges back to  $V_{DD}$ . According to Eq. (4) at this time  $t_{amp}$ , differential output  $\Delta V_0$  has a significant impact on  $t_{latch}$  time. Enhancement in  $\Delta V_0$  lessens the latch time  $t_{latch}$ . From [24],  $\Delta V_0$  of this comparator is calculated as:

$$\begin{aligned} \Delta V_0 &= |V_{out}^+(t = t_{amp}) - V_{out}^-(t = t_{amp})| = \\ &= |V_{thp}| - \frac{I_{B2} \cdot t_{amp}}{C_L} = \\ &= |V_{thp}| \left( 1 - \frac{I_{B2}}{I_{B1}} \right), \end{aligned} \quad (5)$$

where,  $I_{B1}$  and  $I_{B2}$  are the drain currents of the left and right branches of the latch stage. Considering  $\Delta I_B = |I_{B1} - I_{B2}| = g_{mK1,2} \times \Delta V_{F+/F-}$ , Eq. (5) is rewritten as:

$$\Delta V_0 = |V_{thp}| \cdot \frac{\Delta I_B}{I_{B1}} \approx 2|V_{thp}| \cdot \frac{g_{mK1,2} \times \Delta V_{F+/F-}}{I}, \quad (6)$$

where  $g_{mK1,2}$  is the effective trans-conductance of the intermediate PMOS transistors  $M_{K1}$  and  $M_{K2}$  of latch stage and  $\Delta V_{F+/F-}$  is the differential voltage of the pre-amplifier stage output nodes  $F+$  and  $F-$  at the time  $t_{amp}$ . Both these influencing parameters  $g_{mK1,2}$  and  $\Delta V_{F+/F-}$  amplify  $\Delta V_0$  resulting latch delay reduces.

The voltage difference at nodes  $F+/F-$  at time  $t_{amp}$ ,  $\Delta V_{F+/F-}$  can be determined as:

$$\begin{aligned} \Delta V_{F+/F-} &= |V_{F+}(t = t_{amp}) - V_{F-}(t = t_{amp})| = \\ &= t_{amp} \cdot \frac{I_{N1} - I_{N2}}{C_{L,F+(-)}} = \\ &= t_{amp} \cdot \frac{g_{m1,2} \cdot \Delta V_{in}}{C_{L,F+(-)}}. \end{aligned} \quad (7)$$

In this equation,  $I_{N1}$  and  $I_{N2}$  are the currents of input transistors of which difference depends on the input voltage difference i.e.  $\Delta I_B = g_{m1,2} \times \Delta V_{in}$  and  $g_{m1,2}$  is the trans-conductance of the input transistors  $M_1/M_2$ . By substituting Eq. (7) in Eq. (6), we have:

$$\Delta V_0 = \left( \frac{2|V_{thp}|}{I} \right)^2 \times \frac{C_L}{C_{L,F+(-)}} \times g_{mK1,2} \times g_{m1,2} \times \Delta V_{in}. \quad (8)$$

- *Enhancement in effective trans-conductance:* In proposed comparator, it is evident that the output nodes  $F+/F-$  of input stage discharge in decision making phase, ensuing turns on intermediate stage transistors and strengthens positive feedback, thus the effective trans-conductance of the latch is increased i.e.  $(g_{m,eff} + g_{mK1,2})$ . Hence,  $\tau = \frac{C_L}{g_{mK1,2} + g_{m,eff}}$ , and:

$$t_{latch} = \frac{C_L}{(g_{mK1,2} + g_{m,eff})} \cdot \ln \left( \frac{\frac{V_{DD}}{2}}{\Delta V_0} \right). \quad (9)$$

Finally, including effects of both parameters, the total delay of proposed comparator is derived

from:

$$\begin{aligned} t_{delay} &= t_{latch} + t_{amp} = \\ &= \frac{2C_L \cdot |V_{thp}|}{I} + \frac{C_L}{(g_{mK1,2} + g_{m,eff})} \times \\ &\ln \left( \frac{\frac{V_{DD}}{2}}{\left( \frac{2|V_{thp}|}{I} \right)^2 \frac{C_L}{C_{L,F+(-)}} \cdot g_{mK1,2} \cdot g_{m1,2} \cdot \Delta V_{in}} \right). \end{aligned} \quad (10)$$

From expression derived in Eq. (10), it can be concluded that total delay strongly depends on input voltage difference, supply current, trans-conductance of input and intermediate stage transistors, and the ratio of  $C_L$  and  $C_{L,F+(-)}$ . These parameters reduce delay logarithmically and amplify the whole speed of proposed comparator which can be confirmed by the simulation results.

### 2.3. Mismatch Analysis

In the proposed comparator, two intermediate PMOS transistors ( $M_{K1}$  and  $M_{K2}$ ) are included with two phase dynamic comparator [30], thus mismatch effect of threshold voltage ( $\Delta V_{ThK1,2}$ ) and current factor ( $\Delta \beta_{K1,2}$ ) due to  $M_{K1}/M_{K2}$  transistors is considered for input offset analysis. However, the threshold voltage and current factor mismatch effect is insignificant in most cases except small differential input voltage ( $\Delta V_{in}$ ), where output nodes of input stage  $F+$  and  $F-$  follows each other at similar discharge rate. As a result, the decision making outcome might be disturbed due to the mismatch of intermediate transistors. Therefore, following two brief analysis of mismatch effects, caused by threshold voltage and current factor, have been considered on the input offset voltage.

- *Effect of Threshold Voltage Mismatch of  $M_{K1}$  and  $M_{K2}$  ( $\Delta V_{ThK1,2}$ ):* The differential current caused by the  $M_{K1}/M_{K2}$  threshold mismatch is achieved as:

$$\Delta I_B = g_{mK1,2} \times \Delta V_{ThK1,2}. \quad (11)$$

Hence, the input offset voltage caused by the  $M_{K1}/M_{K2}$  threshold mismatch is calculated as follows:

$$\Delta V_{eq, due \Delta V_{ThK1,2}} = \frac{C_{L,F+(-)}}{t_{amp} \cdot g_{m1,2}} \cdot \Delta V_{ThK1,2}. \quad (12)$$

- *Effect of Current Factor Mismatch of  $M_{K1}$  and  $M_{K2}$  ( $\Delta \beta_{K1,2}$ ):* The current factor mismatch of  $M_{K1}/M_{K2}$  can be obtained as channel length mismatch  $\Delta W_{K1,2}$ . In order to find input offset voltage due to current factor mismatch, the differential

current in terms of  $\Delta W_{K1,2}$  can be written as:

$$\Delta I_B = \frac{1}{2} \mu_p \cdot C_{ox} \cdot \frac{\Delta W_{K1,2}}{L} \cdot (V_{gsK1,2} - V_{ThK1,2})^2. \quad (13)$$

Hence, the input offset voltage caused by the  $M_{K1}/M_{K2}$  current factor mismatch is calculated as follows:

$$\begin{aligned} \Delta V_{eq, due \Delta \beta_{K1,2}} &= \frac{\Delta I_B \cdot C_{L,F+(-)}}{t_{amp} \cdot g_{mk1,2} \cdot g_{m1,2}} = \\ &= \frac{0.5 \mu_p \cdot C_{ox} \cdot C_{L,F+(-)}}{t_{amp} \cdot g_{mk1,2} \cdot g_{m1,2}} \times \frac{\Delta W_{K1,2}}{L} \times \\ &\quad \times (V_{gsK1,2} - V_{ThK1,2})^2. \end{aligned} \quad (14)$$

Thus, the total input offset due to both mismatch factors of the intermediate transistors  $M_{K1}/M_{K2}$  can be determined as:

$$\sigma_{total} = \sqrt{\sigma_{\Delta V_{ThK1,2}}^2 + \sigma_{\Delta \beta_{K1,2}}^2}. \quad (15)$$

Expressions derived in Eq. (12) and Eq. (14) conclude that the trans-conductance of input transistors ( $g_{m1,2}$ ) is effective to diminish input offset. So, the size of these input transistors is kept usually large in reducing the effect of intermediate transistors mismatch, which results in low input offset voltage.

## 2.4. Kickback Noise

In the regenerative latched based dynamic comparators, the voltage discrepancy at the output nodes, coupled to input stage transistors, can disturb the input voltage due to nonzero output impedance. This effect, known as kickback noise, may affect the comparator accuracy. As explained in [10], the high speed and low power comparators create larger disturbance at the input nodes. Hence, it is inescapable in the fast latching circuits. In Fig. 3, the undesired peak errors are depicted in the transient response of input voltage at  $\Delta V_{in} = 10$  mV. To determine kickback noise, the Thevenin equivalent of input is modeled with resistance of 8 k $\Omega$ . Figure 4 illustrates the peak error in the input voltage as a function of input voltage difference for three different structures. The proposed comparator has higher kickback noise than two phase dynamic [30] while lower than conventional [27]. The intermediate transistors of proposed circuit are not as robust as latch of two phase dynamic. Thus, the size of these transistors is determined in such a way that the proposed circuit maintains high switching speed and low power dissipation with reduced kickback noise.

The disturbance at reference voltages is negligible as compared to inputs due to low impedance at reference nodes. The main discrepancy occurs during amplification phase when reference voltage takes some level

settling time before the start of regeneration phase. In some applications, in order to reduce the kickback noise where it becomes significant, the kickback noise reduction techniques, such as neutralization in [10], can be applied. The proposed comparator is simulated with neutralization technique as shown in Fig. 4.

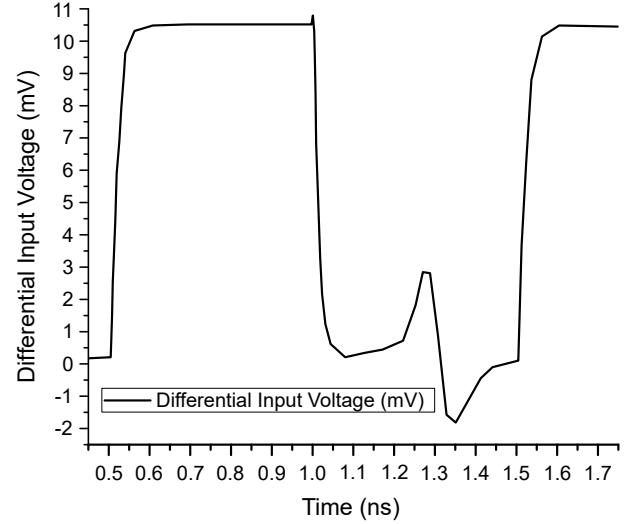


Fig. 3: Undesired peak errors in the input voltage at  $\Delta V_{in} = 10$  mV and  $V_{DD} = 1$  V.

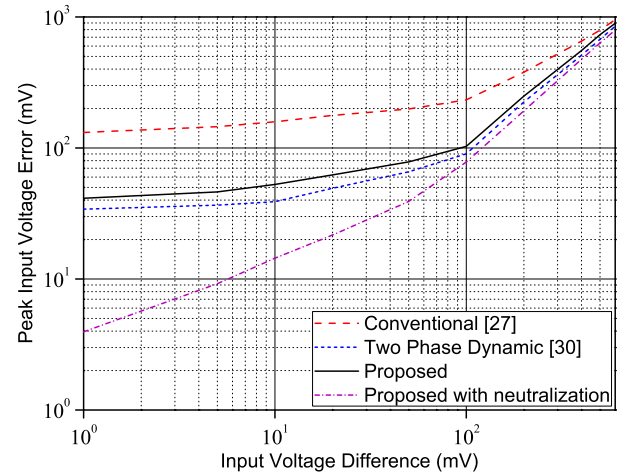


Fig. 4: The plot of measured peak error in input voltage due to kickback noise versus input voltage difference variation.

## 3. Design Considerations

In the proposed structure, there are several design issues that must be considered. The sizing of cross-coupled PMOS transistors  $M_{K1}/M_{K2}$ , located between cross-coupled inverters of latch stage, is an important issue for high speed, low voltage, and low offset operations. These transistors may create the voltage headroom problem, limiting the low voltage applications. In



order to overcome this problem,  $M_{K_1}/M_{K_2}$  transistors of low resistance, i.e. of large size, are required. The input offset might be affected by the threshold voltage and current factor mismatch between  $M_{K_1}/M_{K_2}$  transistors. To diminish this effect,  $M_{K_1}/M_{K_2}$  transistors of large transconductance are required. Therefore, large transistors must be used. However, the large size transistors affect the parasitic capacitances of  $F+/F-$  nodes,  $C_{L,F+(-)}$ , and resulting delay bottlenecks. As, the increased parasitic capacitances restrict the speed of comparator, the size of the  $M_{K_1}/M_{K_2}$  transistors is optimally selected in such a way that maintains the high speed, low voltage, and low offset operations.

In the proposed comparator,  $CLK_1$  and  $CLK_2$  are designed as unbalanced clocks.  $CLK_2$  is delayed by  $\Delta t$  time from  $CLK_1$ , and amplification delay ( $t_{amp}$ ) depends on this delay time ( $\Delta t$ ). So, the design of clock generation circuit is another important issue. As depicted in Fig. 5(a), the delay of  $CLK_2$  with respect to  $CLK_1$  is controlled by varying  $V_{ctrl}$  of the current inverters in the clock buffers. At small  $\Delta V_{in}$ , the comparison is very difficult in evaluation phase. Therefore, in amplification phase, the sufficient amplification time ( $t_{amp}$ ) is required to develop the differential output voltage at the internal nodes  $F+/F-$ . Thus,  $\Delta t$  time is set such that it is equal to or greater than  $t_{amp}$  ( $\Delta t \geq t_{amp}$ ). If  $\Delta t < t_{amp}$ , it will create the error in comparison phase for small  $\Delta V_{in}$ . At higher values of  $\Delta t$ , the input offset is reduced effectively. However, the delay is increased rapidly. Hence, to maintain the high speed and low input offset,  $\Delta t$  is kept equal to or slightly greater than  $t_{amp}$ . For proposed circuit,  $\Delta t = t_{amp}$ . The conceptual waveforms are shown in Fig. 5(b).

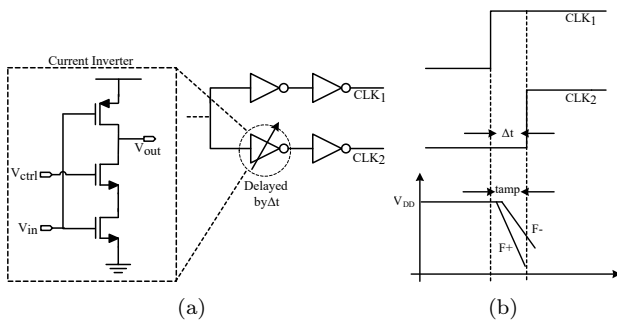


Fig. 5: (a) Clock generation circuit, (b) Conceptual waveform.

## 4. Simulation Results and Discussion

To compare the proposed comparator with existing conventional [27] and two phase dynamic comparator [30], the circuit is designed in CADENCE and

results are simulated in SPECTRE at 90 nm CMOS technology with  $V_{DD} = 1$  V,  $V_{CM} = 0.9$  V and  $\Delta V_{in} = 5$  mV. For fair and authentic comparison of simulation results, the designed circuits from [27] and [30] are simulated in alike simulation environment and framework which is used to simulate the proposed circuit. Figure 6 shows the layout of proposed circuit with area occupancy  $64.08 \mu m^2$  ( $9 \mu m \times 7.12 \mu m$ ). The appropriate caution has been taken in layout design to avoid effect on power, offset and delay. Figure 7 shows the dependence of delay on power supply for proposed comparator and results are compared with other two configurations. It is obvious that speed is significantly enhanced in comparison to other circuits. However, delay is higher at low supply voltages in respect of higher voltage supplies. The delay varies from 364.3 pS to 221 pS for power supply 0.7 V to 1.2 V. Figure 8 and Fig. 9 demonstrate the variation of  $T_{Delay}$  and  $T_{Latch}$  with  $V_{DD}$  at different values of differential input voltage. The values of  $\Delta V_{in}$  are set as 1 mV, 5 mV, 10 mV, 50 mV and 100 mV. It is obvious that  $T_{Delay}$  and  $T_{Latch}$  at particular  $V_{DD}$  are reduced as  $\Delta V_{in}$  is increased. At  $V_{DD} = 1.1$  V, total delay is dropped from 334.59 pS at  $\Delta V_{in} = 1$  mV to 168.87 pS at  $\Delta V_{in} = 100$  mV whereas latch delay drops down from 217.08 pS to 51.36 pS. Also,  $T_{Delay}$  and  $T_{Latch}$  at particular  $\Delta V_{in}$  are decreased as  $V_{DD}$  is increased. At  $\Delta V_{in} = 10$  mV,  $T_{Delay}$  lessens from 272.28 pS at  $V_{DD} = 0.7$  V to 186.46 pS at  $V_{DD} = 1.2$  V and  $T_{Latch}$  from 132.04 pS to 71.33 pS.

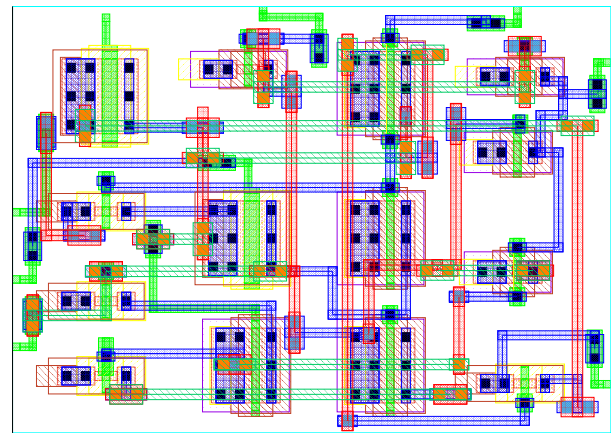


Fig. 6: Layout schematic diagram of proposed comparator (Area =  $9 \mu m \times 7.12 \mu m$ ).

In Fig. 10, the analytical outcomes from Eq. (10) are compared with simulated values of delay at different  $\Delta V_{in}$  and  $V_{CM} = V_{DD} - 0.1$  V. The delay calculated from analytical derivations shows good matching with delay from simulations. The negligible difference is found which is due to non-linear second order effects. These effects are approximated and neglected during analytical derivations of delay to convert the complex expressions into simple expressions.

Figure 11 and Fig. 12 depict the dependency of  $T_{Delay}$  and  $T_{Latch}$  on input voltage difference and results are compared with previous structures. Here,  $\Delta V_{in}$  varies from 1 mV to 30 mV at  $V_{DD} = 1$  V,  $V_{CM} = 0.9$  V and load capacitance,  $C_L$  is 5 fF. At  $\Delta V_{in} = 20$  mV,  $T_{Delay}$  for proposed circuit is 190.63 pS while 298.6 pS and 197.67 pS for conventional design and two phase dynamic circuit, respectively. These results confirm that the delay is reduced for proposed comparator in comparison with past comparators. Also, a significant speed is enhanced compared to conventional circuit. The reason behind the speed improvement is a boost in  $\Delta V_0$ . As shown in Fig. 13,  $\Delta V_0$  variation is represented with  $\Delta V_{in}$ . As  $\Delta V_{in}$  is increased from 1 mV to 30 mV,  $\Delta V_0$  amplifies fast at small differential input and becomes approximately constant at higher values of  $\Delta V_{in}$  which confirms the delay is reduced minimally at large values of  $\Delta V_{in}$ . It also depicts that  $\Delta V_0$  is heightened at particular value of  $\Delta V_{in}$  for proposed configuration as compared to others. For example, at  $\Delta V_{in} = 10$  mV,  $\Delta V_0$  is boosted to 353 mV whereas 136 mV for conventional circuit. At particular value of  $C_L = 5$  fF and  $V_{DD} = 1$  V,  $\Delta V_0$  increases by 225 mV, from 190 mV to 415 mV for  $\Delta V_{in}$  variation from 1 mV to 30 mV.

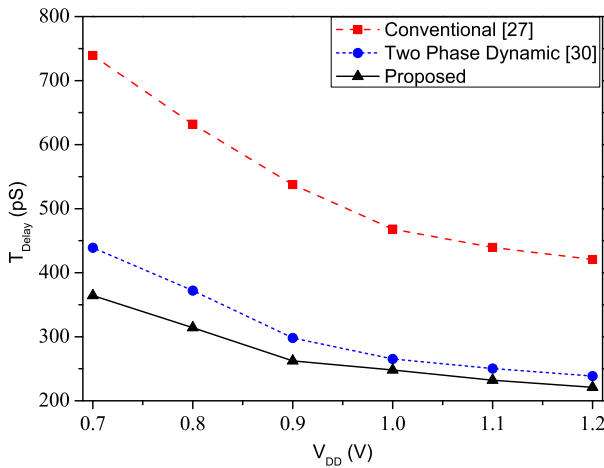


Fig. 7: Total delay for different structures versus  $V_{DD}$  at  $\Delta V_{in} = 5$  mV,  $V_{CM} = V_{DD} - 0.1$  V.

Figure 14 represents that slew rate depends on  $\Delta V_{in}$ . Slew rate increases with increment of  $\Delta V_{in}$  and has larger values for proposed circuit than other circuits. The slew rate is defined as change in output voltage with respect to time ( $\Delta V_0/\Delta t$ ). It proves that slew rate will be higher at small delay time. Slew rate at  $\Delta V_{in} = 5$  mV is  $4.03 \text{ V} \cdot \text{nS}^{-1}$  which is much greater than  $2.14 \text{ V} \cdot \text{nS}^{-1}$  for conventional structure. The whole simulated results conclude that delay is significantly reduced with comparable power dissipation,  $P_{diss}$  as shown in Fig. 15.  $P_{diss}$  at  $\Delta V_{in} = 10$  mV is  $44.97 \text{ } \mu\text{W}$  for proposed which is comparable to  $43.79 \text{ } \mu\text{W}$  for two phase dynamic. Moreover,  $P_{diss}$  is significantly lower

than that of conventional circuit at every particular value of  $\Delta V_{in}$ . For example,  $P_{diss} = 53.36 \text{ } \mu\text{W}$  at  $\Delta V_{in} = 5$  mV for proposed, on the contrary,  $86.07 \text{ } \mu\text{W}$  for conventional circuit. It is obvious that speed is expressively enhanced while consuming almost same power. Hence Energy Per Conversion (EPC) [24] is reduced which is defined as  $EPC = \frac{P_{diss}}{2^{ENOB} \cdot f_s}$ , where ENOB is effective number of bits and  $f_s$  is sampling frequency.

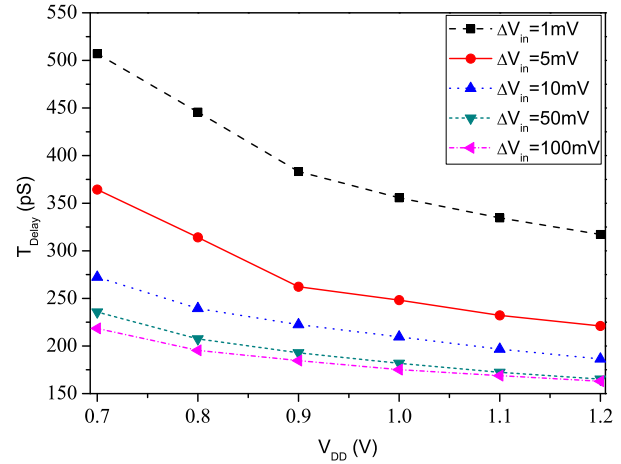


Fig. 8: Total delay for proposed comparator versus  $V_{DD}$  at various  $\Delta V_{in}$  ( $V_{CM} = V_{DD} - 0.1$  V).

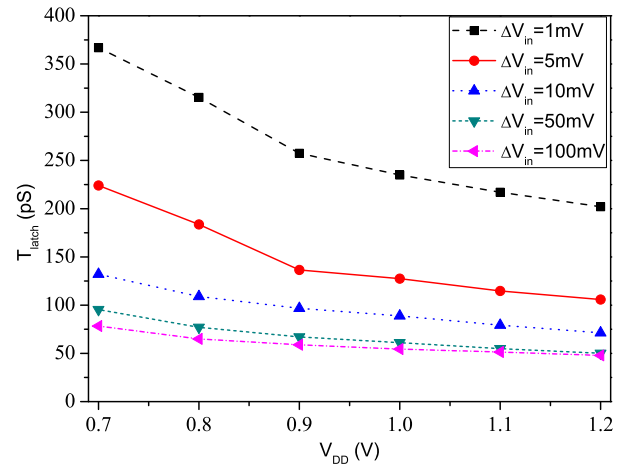
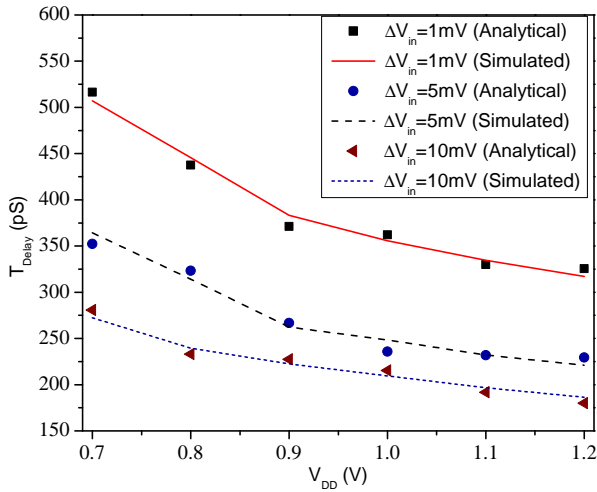


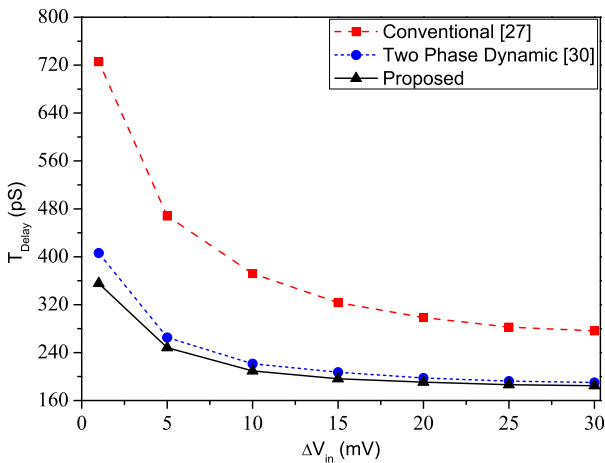
Fig. 9: Latch delay for proposed comparator versus  $V_{DD}$  at various  $\Delta V_{in}$  ( $V_{CM} = V_{DD} - 0.1$  V).

EPC in proposed circuit is slightly reduced in comparison with two phase dynamic circuit while an impressive drop occurs in respect of conventional circuit as shown in Fig. 16. For 1 bit conversion, EPC is decreased from  $13.25 \text{ fJ}$  to  $3.4 \text{ fJ}$  at  $\Delta V_{in} = 5$  mV after comparing with conventional structure, on the contrary, a slight drop with two phase dynamic from  $2.15 \text{ fJ}$  to  $1.99 \text{ fJ}$  at  $\Delta V_{in} = 10$  mV. In Tab. 1, the performance of the proposed structure has been sum-

marized. Table 2 includes and verifies both analytical analysis and 0.2 k Monte Carlo simulated values for offset voltage. There is a small difference in calculated and simulated values. The offset voltage calculated from analytical derivations is lower than the simulated result by meticulous  $1 - \sigma$  Monte Carlo simulations. The small difference is due to the dynamic offset which is not considered in analytical derivations.



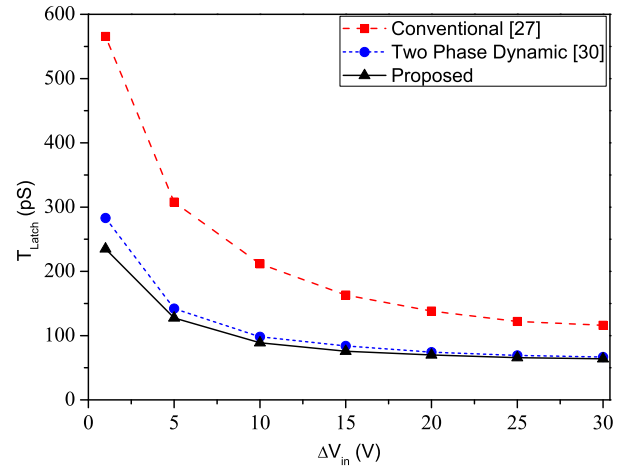
**Fig. 10:** Verification of analytical analysis with simulation results for delay at different  $\Delta V_{in}$  and  $V_{CM} = V_{DD} - 0.1$  V.



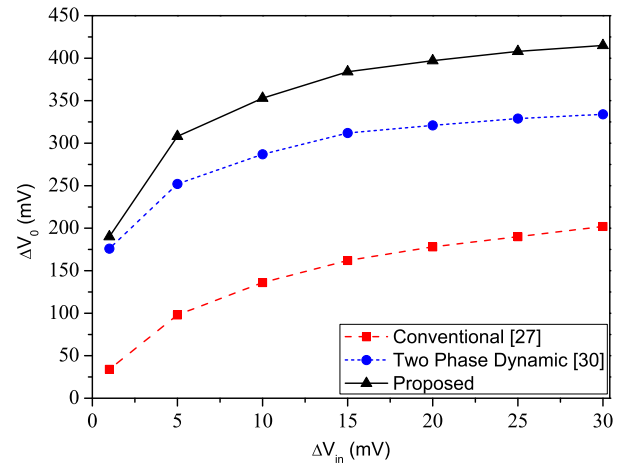
**Fig. 11:** Total delay for different structures versus  $\Delta V_{in}$  at  $V_{DD} = 1$  V,  $V_{CM} = 0.9$  V.

Figure 17 shows the offset voltage variation of current proposed circuit with previous configurations at three different supply voltages. By using unbalanced clock scheme, the input offset is reduced remarkable with respect to conventional, and additions of intermediate transistors lessen somewhat more input offset voltage, but keep in mind that size of these transistors should be larger with respect to others. At  $V_{DD} = 1.2$  V, the input offset voltage ( $V_{os}$ ) is 63.85 mV,

11.67 mV and 8.32 mV for conventional, two phase dynamic and proposed circuit, respectively. At each point, the offset results are achieved using  $1 - \sigma$  Monte Carlo simulations at 200 samples run. As shown in Fig. 18, the standard deviation of the input offset ( $\sigma_{os}$ ) for the proposed circuit is derived to be 10.8 mV at  $V_{DD} = 1$  V using  $1 - \sigma$  based Monte Carlo simulations.



**Fig. 12:** Latch delay for different structures versus  $\Delta V_{in}$  at  $V_{DD} = 1$  V,  $V_{CM} = 0.9$  V.

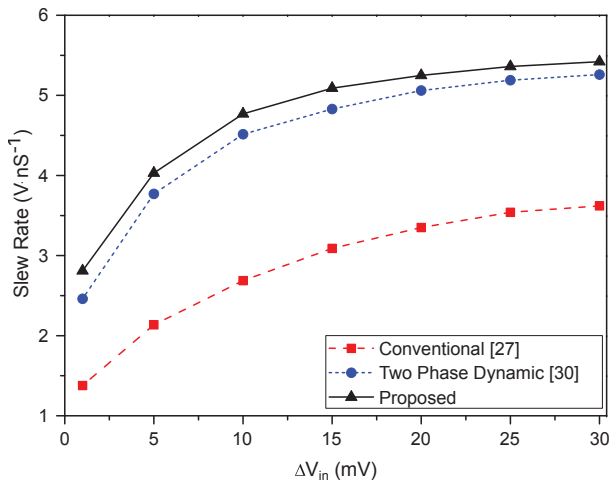


**Fig. 13:**  $\Delta V_0$  (differential output voltage at  $t = t_{amp}$ ) for different structures versus  $\Delta V_{in}$  at  $V_{DD} = 1$  V,  $V_{CM} = 0.9$  V.

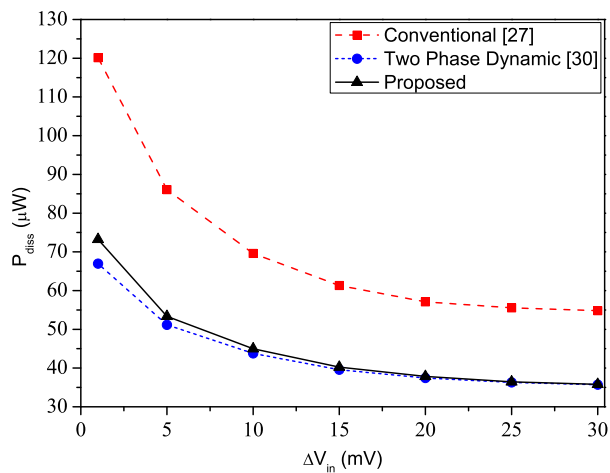
Table 3 presents the corner analysis for proposed comparator at  $\Delta V_{in} = 5$  mV and  $V_{DD} = 1$  V. Thus, the proposed circuit works properly at different corners. However, the delay is increased with some extent at SS corner. To draw a fair comparison, the proposed structure and two other structures from [27] and [30] are simulated and compared in same simulation environment at 90 nm CMOS technology as shown in Tab. 4. The width of the MOS transistors is set such that the optimized values are drawn for delay and off-



set. Finally, Tab. 5 relates the performance parameters of the proposed structure with previous works.



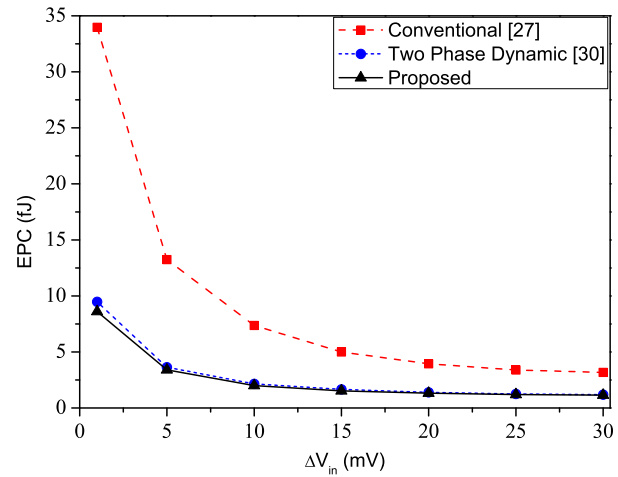
**Fig. 14:** Slew rate for different structures versus  $\Delta V_{in}$  at  $V_{DD} = 1$  V,  $V_{CM} = 0.9$  V.



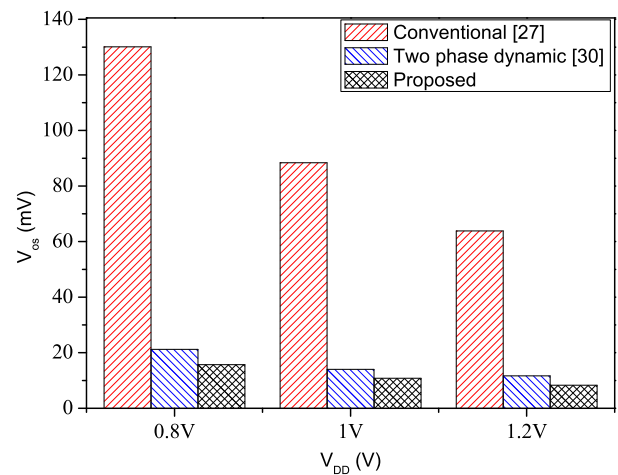
**Fig. 15:** Power dissipation for different structures versus  $\Delta V_{in}$  at  $V_{DD} = 1$  V,  $V_{CM} = 0.9$  V.

**Tab. 1:** Proposed Comparator Performance Summary.

Parameters	Values
CMOS Technology	90 nm
Supply Voltage	1 V
Total Delay, $T_{Delay}$ ( $V_{CM} = 0.9$ V, $\Delta V_{in} = 5$ mV)	248.2 pS
Latch Delay, $T_{Latch}$	127.53 pS
Differential Output Voltage at $t_{amp}$ ( $\Delta V_0$ )	308 mV
Average Power Dissipation @ freq. = 0.5 GHz	53.36 $\mu$ W
Maximum Sampling Frequency	5.7 GHz
Slew Rate	4.03 V-nS <sup>-1</sup>
Energy Per Conversion @ $\Delta V_{in} = 5$ mV	3.4 fJ
Input Offset Voltage ( $1 - \sigma$ ) ( $\sigma_{os}$ )	10.8 mV



**Fig. 16:** EPC for different structures versus  $\Delta V_{in}$  at  $V_{DD} = 1$  V,  $V_{CM} = 0.9$  V.



**Fig. 17:** Input offset for different structures versus  $V_{DD}$  at  $\Delta V_{in} = 5$  mV,  $V_{CM} = V_{DD} - 0.1$  V.

**Tab. 2:** Validation of analytical analysis with simulated values of offset voltage.

$V_{DD}$ (V)	$\Delta V_{in} = 1$ mV		$\Delta V_{in} = 5$ mV	
	Simulated Value (mV)	Analytical Value (mV)	Simulated Value (mV)	Analytical Value (mV)
0.8	12.32	10.95	16.81	15.7
1.0	8.79	7.41	11.56	10.8
1.2	6.98	6.03	9.12	8.32

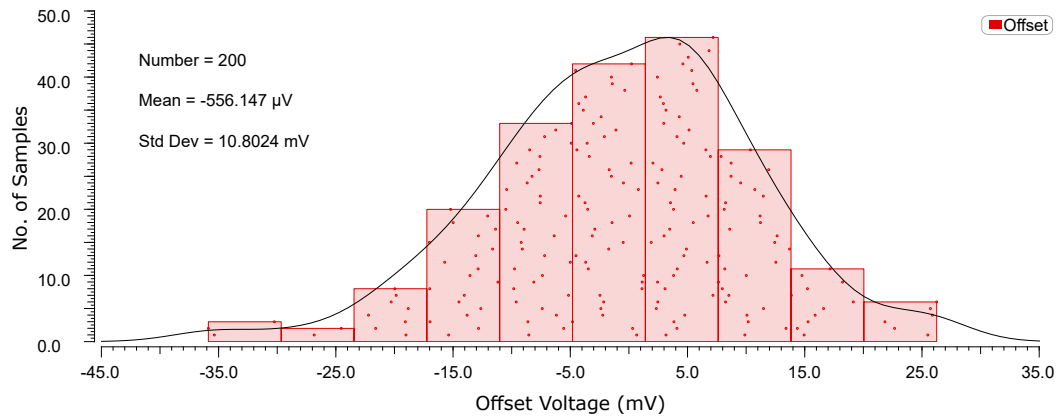
**Tab. 3:** Performance summary of proposed comparator at different corners.

Corners	Parameters			
	Delay (pS)	Power ( $\mu$ W)	$1 - \sigma$ Offset (mV)	EPC (fJ)
TT	248.2	53.36	10.8	3.39
FF	212.6	56.94	8.9	3.01
FS	273.8	50.23	13.3	3.47
SF	262.4	51.87	11.7	3.42
SS	325.1	48.35	15.4	3.96

**Tab. 4:** Performance comparison with conventional and two phase dynamic comparator in same simulation environment.

Parameters		[27]	[30]	Proposed
Maximum Sampling Frequency (GHz)		1	3.9	5.7
Total Delay, $T_{Delay}$ (pS) @ $\Delta V_{in} = 5$ mV		468.2	265.3	248.2
Input Offset Voltage, $\sigma_{os}$ (mV)	$\Delta V_{in} = 1$ mV	67.5	11.22	7.41
	$\Delta V_{in} = 5$ mV	88.4	14.01	10.8
Kickback Noise Voltage (mV) @ $\Delta V_{in} = 10$ mV	Without Neutralization	158.64	38.93	52.64
	With Neutralization	67.37	7.25	14.43
Average Power Dissipation ( $\mu$ W) @ $\Delta V_{in} = 5$ mV		86.07	51.16	53.36
EPC (fJ) @ $\Delta V_{in} = 5$ mV		13.25	3.63	3.4
Area ( $\mu\text{m}^2$ )		77.34	58.62	64.08

$$V_{DD} = 1 \text{ V}, V_{CM} = 0.9 \text{ V}, f_{CLK} = 0.5 \text{ GHz @ } 90 \text{ nm CMOS process}$$

**Fig. 18:** Histogram of input offset voltage for proposed comparator achieved at 0.2 k Monte Carlo simulations.**Tab. 5:** Performance comparison with previous work.

Parameters		[6] <sup>a</sup>	[8] <sup>b</sup>	[24] <sup>a</sup>	[27] <sup>a</sup>	[30] <sup>a</sup>	[32] <sup>a</sup>	[33] <sup>a</sup>	[34] <sup>a</sup>	Proposed <sup>a</sup>
CMOS Technology (nm)		180	40	180	90	90	130	90	180	90
Supply Voltage (V)		1.8	1.1	1.2	1	1	1.2	1	1.8	1
Clock Frequency (GHz)		0.05	6	0.5	*	*	*	*	0.1	0.5
Max. Sampling Frequency (GHz)		0.05	16.4	2.4	1	1	*	3	0.1	5.7
Total Delay (pS)		4200	61.08	550	550	152	Calibration Time 400 ns	170	*	248.2
Offset Voltage (mV)		3.44	*	7.8	102	33	100/0.22	16.3	*	10.8 @ $\Delta V_{in} = 5$ mV
										7.41 @ $\Delta V_{in} = 1$ mV
Kickback Noise Voltage (mV) @ $\Delta V_{in} = 10$ mV	Without Neutralization	*	*	43	*	*	*	*	*	52.64
	With Neutralization	*	*	13	*	*	*	*	*	14.43
Average Power Dissipation ( $\mu$ W)		158.5	345.9	329	60	51	4080	162	900	53.36
Energy Per Conversion (fJ)		0.7	57.65	240	*	*	*	59.2	*	3.4
Area ( $\mu\text{m}^2$ )		8883.36	64.5	392	3.84	3.3	*	*	*	64.08

<sup>a</sup> Simulation Results, <sup>b</sup> Measurement Results, \* Not Reported

## 5. Conclusion

In this paper, a novel unbalanced clock based dynamic comparator has been presented to diminish latch regeneration delay and offset. The latch stage is modified by adding two intermediate transistors which enhances the regeneration speed. The unbalanced clock signaling aids to cancel the mismatch effect of the interior devices. The analytical derivations for the proposed comparator are presented to analyze delay and offset that verify the results simulated by CADENCE

VIRTUOSO tool. The simulated results confirm the reduction in delay and offset for the proposed circuit as compared to the previous structures. The maximum sampling frequency of proposed comparator is 5.7 GHz at  $V_{DD} = 1$  V with total delay of 248.2 pS and input offset of 10.8 mV at the cost of 53.36  $\mu$ W power consumption and 64.08  $\mu\text{m}^2$  area. The delay is reduced up to 46 % and 6 % as compared to conventional and two phase dynamic comparator, respectively. The offset is also minimized by 88 % and 23 % in comparison of conventional and two phase dynamic comparator, respectively.

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